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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael R. BRUCE t al.

Docket: AMDA.441PA

Title: ELECTRICAL PROBING OF SOI STRUCTURES

CERTIFICATE UNDER 37 CFR 1.10
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☒ Patent Application: Pages Numbered 1-16; 23 claims; Abstract 1 pgs.
☒ 3 sheets of informal drawings
☒ An executed Declaration
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AMDA.441PA (TT3751)
May 30, 2000

ELECTRICAL PROBING OF SOI CIRCUITS

Field of the Invention

The present invention relates generally to semiconductor dies and their fabrication and, more particularly, to analysis of semiconductor dies involving capacitive probing.

Background of the Invention

The semiconductor industry has recently experienced technological advances that have permitted dramatic increases in integrated circuit density and complexity, and equally dramatic decreases in power consumption and package sizes. Present semiconductor technology now permits single-chip microprocessors with many millions of transistors, operating at speeds of hundreds of millions of instructions per second to be packaged in relatively small, air-cooled semiconductor device packages.

A by-product of such high-density and high functionality is an increased demand for products employing these microprocessors and devices for use in numerous applications. As the use of these devices has become more prevalent, the demand for faster operation and better reliability has increased. Such devices often require manufacturing processes that are highly complex and expensive.

As the manufacturing processes for semiconductor devices and integrated circuits increase in difficulty, methods for testing and debugging these devices become increasingly important. Not only is it important to ensure that individual chips are

functional, it is also important to ensure that batches of chips perform consistently. In addition, the ability to detect a defective manufacturing process early is helpful for reducing the number of defective devices manufactured.

Traditionally, integrated circuits have been tested using methods including directly accessing circuitry or devices within the integrated circuit. Directly accessing the circuitry is difficult for several reasons. For instance, in flip-chip type dies, transistors and other circuitry are located in a very thin epitaxially-grown silicon layer in a circuit side of the die. The circuit side of the die is arranged face-down on a package substrate. This orientation provides many operational advantages. However, due to the face-down orientation of the circuit side of the die, the transistors and other circuitry near the circuit side are not readily accessible for testing, modification, or other purposes. Therefore, access to the transistors and circuitry near the circuit side is from the back side of the die.

One particular type of semiconductor device structure that presents unique challenges to back side circuit analysis is silicon-on-insulator (SOI) structure. SOI involves forming an insulator, such as an oxide, over bulk silicon in the back side of a semiconductor device. A thin layer of silicon is formed on top of the insulator, and is used to form circuitry over the insulator. The resulting SOI structure exhibits benefits including reduced switch capacitance, which leads to faster operation. Direct access to circuitry for analysis of SOI structure, however, involves milling through the oxide. The milling process can damage circuitry or other structure in the device. Such damage can alter the characteristics of the device and render the analysis inaccurate. In

addition, the milling process can be time-consuming, difficult to control, and thus expensive.

The difficulty, cost, and destructive aspects of existing methods for testing integrated circuits are impediments to the growth and improvement of semiconductor technologies involving SOI structure.

Summary of the Invention

The present invention is directed to a method and system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure in a manner that addresses and can even overcome the above-discussed impediments. The die includes a back side opposite circuitry in a circuit side, and the die analysis involves coupling to the circuitry. The present invention is exemplified in a number of implementations and applications, some of which are summarized below.

According to an example embodiment of the present invention, a semiconductor die having SOI structure and a back side opposite circuitry in a circuit side is analyzed. A portion of substrate is removed from the back side of the semiconductor die and an exposed region of the insulator portion of the SOI die is formed. A detectable response is induced from the exposed region as a function of a portion of the circuitry. Detecting a response from the die in this manner expedites and enhances analysis of semiconductor devices that employ SOI construction, thereby improving the manufacture, testing, and technological advancement of such devices.

In another example embodiment of the present invention, an electron beam is directed at the exposed region in the semiconductor die using, for example, a scanning

electron microscope (SEM). The electron beam generates secondary electrons in the exposed region that are detected and used to analyze the die. Such generation of secondary electrons occurs as a function of an electrical characteristic of a portion of the circuitry in the die. This functional relationship between the generation of secondary electrons and the electrical characteristic of the circuitry is used to analyze the die.

According to another example embodiment of the present invention, a system is adapted to analyze a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry in a circuit side. The system includes a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and form an exposed region in the insulator portion of the SOI structure. A probe arrangement is adapted to induce a detectable response from the exposed region as a function of a portion of the circuitry. A detector is adapted to detect the response and to analyze the die therefrom.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and detailed description that follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 is a semiconductor die having SOI structure for use in connection with the present invention;

FIG. 2 is a semiconductor die undergoing analysis, according to an example embodiment of the present invention; and

FIG. 3 is a system for analyzing a semiconductor die, according to another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not necessarily to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is believed to be applicable to a variety of different types of semiconductor devices, and has been found to be particularly suited for flip-die and other type devices having silicon-on-insulator (SOI) structure and requiring or benefiting from analysis involving obtaining a response from the insulator portion of the SOI structure. While the present invention is not necessarily limited to such devices, various aspects of the invention may be appreciated through a discussion of various examples using this context.

According to an example embodiment of the present invention, a semiconductor die having a back side opposite circuitry in a circuit side and including SOI structure is analyzed using a response detected from the insulator portion as a function of circuitry in the die. First, a portion of substrate is removed from the back side of the die, and an

exposed region of the insulator of the SOI die is formed over circuitry in the circuit side. It has been unexpectedly discovered that, using the insulator, for example, an electron beam on a probe can be used to image a response from the dielectric to analyze the underlying circuitry. In this manner, electrical characteristics are obtained from the circuitry and used to analyze the die. The analysis can be used, for example, to determine die logic states for post-manufacturing analysis.

FIG. 1 shows a portion of a flip die die 100 exemplifying one type of a variety of dies having SOI structure to which the present invention is applicable. The die of FIG. 1 is shown in an inverted position with the back side facing up, such as would be a flip die bonded to a package substrate. A very thin buried oxide (BOX) 150 is formed over silicon substrate 160, and a thin layer of silicon 140 is formed on the oxide 150. Source/drain regions 120 and 130 are formed in the thin layer of silicon 140. A gate 110, formed over the thin layer of silicon 140 and an intervening gate insulator layer 142, is used together with the source/drain regions to create a SOI transistor.

FIG. 2 shows a semiconductor die having SOI structure, such as shown in FIG. 1, undergoing analysis in accordance with another example embodiment of the present invention. A portion of silicon substrate 260 has been removed from the back side of the die 200, leaving a exposed probe surface 270 of a BOX layer 250. The substrate can be removed, for example, using typically-available substrate removal methods and devices, such as using a focused ion beam (FIB), a laser etching device, or an etch chamber having an etch gas and used in combination with a masking step. In one particular example embodiment (not illustrated), the back side silicon substrate is

globally thinned using a polishing process, such as chemical-mechanical polishing, and is followed by a locally thinning process.

The probe surface 270 is shown on the BOX 250 in this example embodiment. However, the probe surface may be created in any manner sufficient to permit an electrical characteristic of a portion of circuitry in the die to be probed. For example, the probe surface may be formed in the substrate 260, wherein the amount of the substrate that has been removed creates an opening that is sufficiently deep to facilitate the capacitive coupling. In another example, a portion of the BOX 250 is removed and the probe surface 270 is created in the BOX 250, with the depth similarly chosen to facilitate the probing. A cold finger (plate) can be applied to one or more selected locations on the die to maintain the die temperature.

After the probe surface 270 has been defined, a probing arrangement is used to induce a response that is a function of underlying circuit regions in the die. Transistors 210 and 220, separated by isolation region 205, are shown undergoing electron beam probing. First, an electron beam 230 is directed at a portion of the probe surface over a source/drain region 212 of transistor 210. The beam can be directed at selected regions by imaging the circuitry through the BOX and navigating to the selected region using the image, or using other typically available navigation methods. In one implementation, the electron beam is generated and controlled using a scanning electron microscope (SEM). The BOX 250 acts as a dielectric and facilitates capacitive coupling between the probe region and the source/drain region. Secondary electrons 235 are emitted in response to the electron beam and are modulated by electric fields in the BOX. In this instance, the electric field generated by the source/drain region 212

affects the emission of secondary electrons. If the source/drain region is at a positive voltage, such emission of secondary electrons is inhibited, and if the voltage is zero or negative, the emission of secondary electrons is generally unaffected. This variation in secondary electron emission is used to detect an electrical characteristic from the transistor 210.

The beam 230' is then caused to scan the transistor 220 and probe source/drain region 222 in a similar manner to which source/drain region 212 was probed. Secondary electrons 235' are emitted from source drain region 222 and used to detect an electrical characteristic from the region 222. As shown, the emission of secondary electrons 235' is inhibited as compared to secondary electrons 235. This inhibited emission is detected and used to detect that the two transistors exhibit different characteristics. In this instance, source/drain region 222 has a higher positive voltage than source/drain region 212. The inhibited secondary electron response from source/drain region 222 is detected and used to determine that it is at a higher positive voltage. If desired, various other circuit portions of the die can be analyzed using the same technique, and responses can be used to detect variations in voltage across the die. The responses can then be used to create an image representing the voltage states of the die. For more information regarding capacitive coupling, probing and the detection of secondary electrons, reference may be made to Christopher G. Talbot, *Probing Technology for IC Diagnosis, in* FAILURE ANALYSIS OF INTEGRATED CIRCUITS 113, (Lawrence C. Wagner ed., 1999).

In another example embodiment of the present invention, a non-defective die is analyzed in the same manner as described hereinabove. Response data from the die can

be obtained for one or several circuit elements to be subsequently analyzed in a defective die. The data from the non-defective die is then stored and compared with data obtained from the defective die. In one particular implementation, a series of test vectors are input to the non-defective die. The same signals are input to the defective die, and the response is compared. Variations in the response can be used to detect that the defective die is not operating properly.

According to another example embodiment of the present invention, FIG. 3 shows a system 300 arranged to probe a semiconductor die 301 having SOI structure, such as the die shown in FIGs. 1 and 2. The die 301 is located on a die holder 310. A electron beam generator 320 is adapted to direct an electron beam 322 at an exposed probe region in the die 301. The beam 322 induces a response from the die via the BOX that is a function of underlying circuitry in the die. A detector 330 is adapted to detect secondary electrons 332 emitted from the die 301 in response to the electron beam 322. The detected secondary electrons are used to detect an electrical characteristic of the die 301, such as described hereinabove. In one implementation, the die holder 310, beam generator 320 and detector 330 are part of a single SEM arrangement, shown by dashed lines 370.

The system 300 optionally includes a controller adapted to control the probe, such as a computer arrangement 340. In one implementation, the computer arrangement is adapted to receive electrical characteristics of the die 301 via the detector 330 and interpret those characteristics to analyze the die. The computer arrangement 340 can also be programmed to control the beam generator 320 for obtaining various results. For instance, the beam can be pulsed rapidly to obtain a

waveform response from the detector. The pulsing can be generated in sequences having a duration in the microsecond, picosecond or even shorter range. This is particularly useful for obtaining waveforms from high frequency applications, and for obtaining a capacitive measurement in response to a particular input signal.

The computer 340 is further optionally coupled to a display 350 adapted to provide information indicative of the response from the detector 330. For example, the display can be used to display a waveform response from the die in the pulsed application described above. In addition, the display can be used to display an image of the die having variations in contrast related to the secondary electrons detected. Portions of the die emitting few secondary electrons (*e.g.*, circuitry having a positive voltage) show up as dark spots, and portions emitting greater numbers of secondary electrons show up as bright spots.

In another example embodiment of the present invention, the die 301 is powered for analysis using supply 360. The power supply is coupled to the die 301 via the holder 310 and is used to input signals to circuit elements in the die. A response to the input signals is obtained by detecting the secondary electrons 332. The input signals may, for example, include normal operating signals supplied to the die, or may include signals known to cause a failure in the die. In one particular implementation, the signals are input in a continuous loop that generates a failure in the die. The response is capacitively monitored and used for analyzing the die.

In another example embodiment of the present invention (not shown), the system 300 includes a substrate removal device adapted to remove substrate from the back side of the die 301 and form an exposed region having a probe area. In one

implementation, the substrate removal device includes a FIB, and in another implementation, the substrate removal device includes a laser etching device. The exposed region is formed having a depth that is sufficient to facilitate inducing a response related to a source/drain region or other circuitry portion in the die, such as by exposing a BOX layer in a SOI structure.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.

What is claimed is:

1. A method for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the method comprising:

removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed; and

inducing a detectable response from the exposed region as a function of a portion of the circuitry and, therefrom, analyzing the die.

2. The method of claim 1, wherein inducing a detectable response includes using an electron beam.

3. The method of claim 2, further including detecting secondary electrons generated in response to the electron beam and the portion of the circuitry and wherein analyzing the die includes using a scanning electron microscope (SEM).

4. The method of claim 3, wherein analyzing the die includes detecting a first magnitude of secondary electrons from a selected circuit portion and a second magnitude of secondary electrons detected from another circuit portion, the first and second magnitudes of secondary electrons being indicative of an electric characteristic differential between the selected circuit portion and the other circuit portion.

5. The method of claim 4, further comprising detecting secondary electrons from a plurality of circuit portions and obtaining an image of the die that represents variations in voltage across the plurality of circuit portions.

6. The method of claim 2, wherein using the electron beam includes pulsing the beam, and wherein analyzing the die includes obtaining a waveform response to the pulsed beam.

7. The method of claim 6, further comprising coupling a power supply to the die and inputting electrical signals to the die to generate a response.

8. The method of claim 1, wherein inducing a detectable response includes inducing a response as a function of an electrical characteristic of a source/drain region in the die.

9. The method of claim 1, wherein inducing a detectable response includes using a buried oxide (BOX) portion of the SOI structure as a dielectric.

10. The method of claim 9, wherein removing a portion of substrate from the back side of the semiconductor die includes exposing a portion of the BOX.

11. The method of claim 1, wherein analyzing the die includes post-manufacturing analysis.

12. The method of claim 11, wherein analyzing the die includes obtaining a response for electrical stimulus applied to circuitry in the die.

13. The method of claim 12, wherein inputting electrical signals includes inputting signals known to induce a failure in the die.

14. The method of claim 12, wherein inputting electrical signals includes inputting signals in a continuous loop.

15. The method of claim 1, further comprising inducing a detectable response from a non-defective die in the same manner as the die being analyzed, the non-defective die having the same design as the die being analyzed, and comparing the analysis of the dies.

16. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

means for removing substrate from the back side of the semiconductor die and exposing a region of the insulator of the SOI structure where the substrate has been removed;

means for inducing a detectable response from the exposed region as a function of a portion of the circuitry; and

means for detecting the response and, therefrom, analyzing the die.

17. A system for analyzing a semiconductor die having silicon-on-insulator (SOI) structure and a back side opposite circuitry near a circuit side, the system comprising:

a substrate removal arrangement adapted to remove substrate from the back side of the semiconductor die and expose a region of the insulator of the SOI structure where the portion has been removed;

a probe arrangement adapted to induce a detectable response from the exposed region as a function of a portion of the circuitry; and

a detector adapted to detect the response and, therefrom, analyze the die.

18. The system of claim 17, further comprising a controller adapted to control the substrate removal arrangement.

19. The system of claim 18, wherein the controller is adapted to control the substate removal arrangement to remove sufficient substrate to facilitate the inducing of a response from the exposed region as a function of a portion of the circuitry.

20. The system of claim 17, wherein the substrate removal arrangement is adapted to remove enough substrate to expose a BOX portion of the SOI structure.

21. The system of claim 17, wherein the probe arrangement includes an SEM adapted to provide at least one of: an image of a circuit under analysis and data for probe navigation.

22. The system of claim 21, wherein the SEM also includes the detector and is further adapted to obtain an image of the die having light and dark areas, the dark areas being indicative of circuit portions having a positive voltage greater than that of lighter areas.

23. The system of claim 17, further comprising a tester adapted to introduce electrical stimulus to the die.

Abstract

Analysis of a semiconductor die having silicon-on-insulator (SOI) structure is enhanced by accessing the circuitry within the die from the back side without necessarily breaching or needing to breach the thin insulator layer of the SOI structure. According to an example embodiment of the present invention, a portion of substrate is removed from the back side of a semiconductor die having a SOI structure and a backside opposite circuitry in a circuit side. An exposed region is formed where the substrate has been removed. A detectable response from the exposed region is induced, for example, by an electron beam, as a function of a portion of the active circuitry within the die.

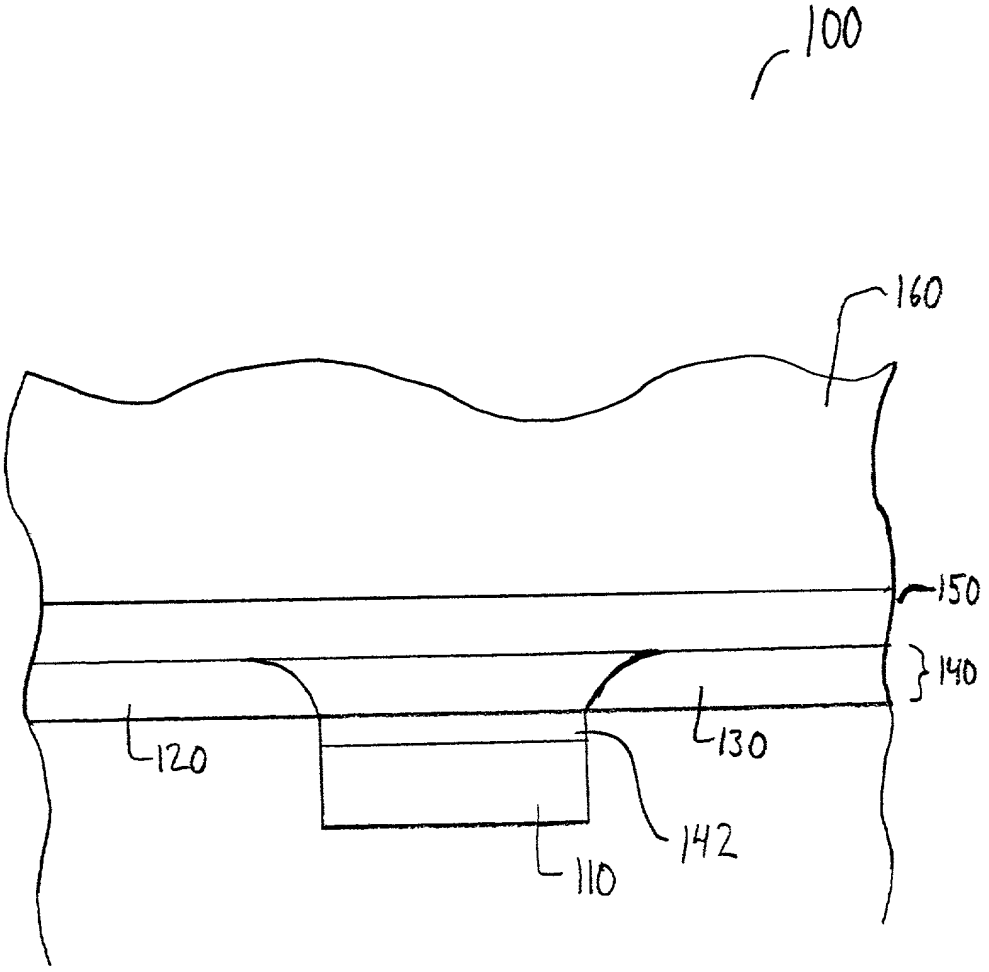

Fig. 1 (Prior Art)

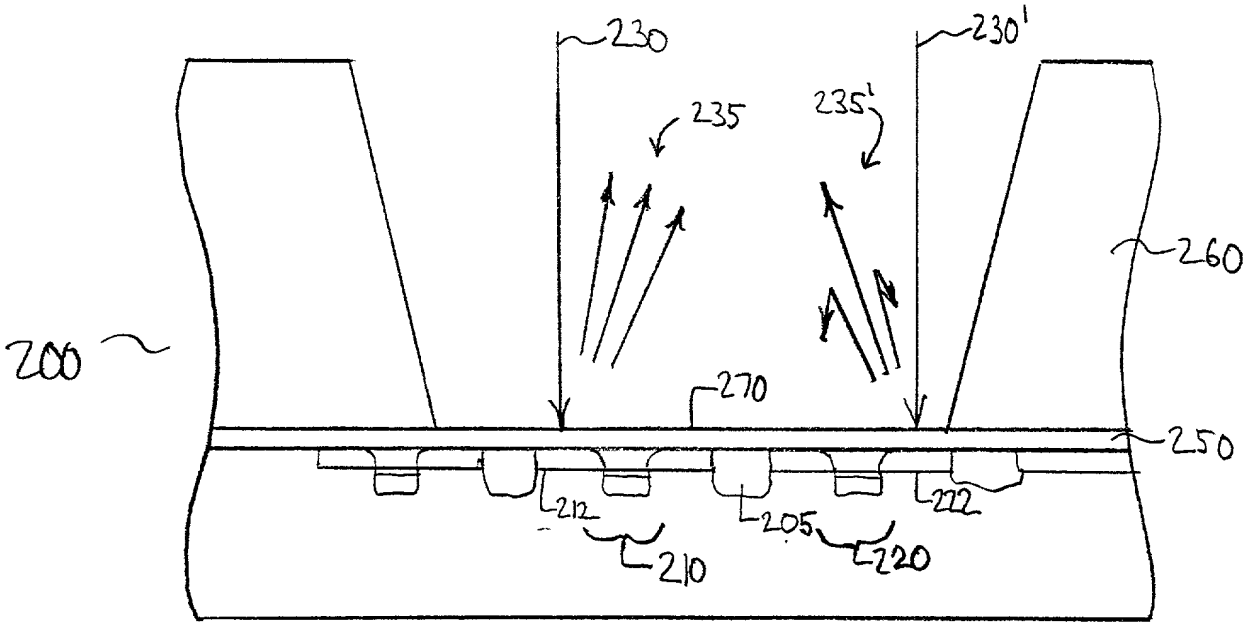

Fig. 2

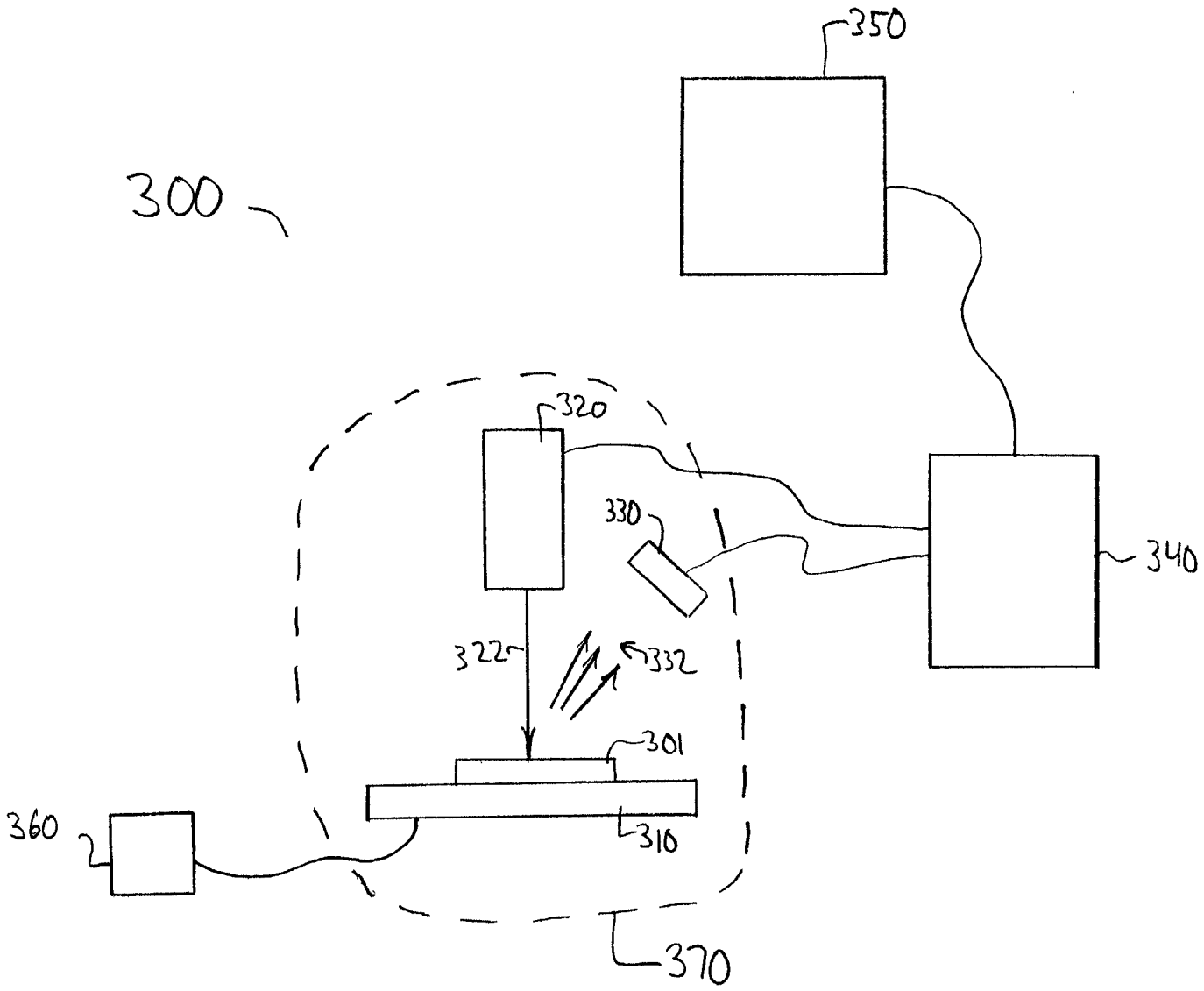

Fig. 3

CRAWFORD PLLC

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **ELECTRICAL PROBING OF SOI CIRCUITS.**

The specification of which
a. ☐ is attached hereto
b. ☒ is entitled **ELECTRICAL PROBING OF SOI CIRCUITS ,** having attorney docket number **AMDA.441PA (TT3751).**
c. ☐ was filed on as application serial no. and was amended on (if applicable) (in the case of a PCT-filed application) described and claimed in international no. filed and as amended on (if any), which I have reviewed and for which I solicit a United States patent.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56 (attached hereto).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

a. ☒ no such applications have been filed.
b. ☐ such applications have been filed as follows:

FOREIGN APPLICATION(S), IF ANY, CLAIMING PRIORITY UNDER 35 USC § 119			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**
ALL FOREIGN APPLICATION(S), IF ANY, FILED BEFORE THE PRIORITY APPLICATION(S)			
COUNTRY	**APPLICATION NUMBER**	**DATE OF FILING (day, month, year)**	**DATE OF ISSUE (day, month, year)**

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. APPLICATION NUMBER	DATE OF FILING (day, month, year)	STATUS (patented, pending, abandoned)

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

U.S. PROVISIONAL APPLICATION NUMBER	**DATE OF FILING** (Day, Month, Year)

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Crawford, Robert J.	Reg. No. 32,122	Jimenez, José W.	Reg. No. 31,113
Maunu, LeRoy D.	Reg. No. 35,274		
Drake, Paul S.	Reg. No. 33,491	Pitruzzella, Vincenzo D.	Reg. No. 28,656
Apperley, Elizabeth A.	Reg. No. 36,428	Roddy, Richard J.	Reg. No. 27,688
Riley, Louis A.	Reg. No. 39,817	Zahrt II, William D.	Reg. No. 26,070

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Crawford PLLC.

Please direct all correspondence in this case to Crawford PLLC at the address indicated below:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

201	**Full Name Of Inventor**	**Family Name** GORUGANTHU	**First Given Name** RAMA	**Second Given Name** R.
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Signature of Inventor 201: Rama Goruganthu			**Date:** 5/30/00	
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Signature of Inventor 202: Michael Bruce			**Date:** 5/30/00	
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210	**Residence & Citizenship**	**City**	**State or Foreign Country**	**Country of Citizenship**
213	**Post Office Address**	**Post Office Address**	**City**	**State & Zip Code/Country**
Signature of Inventor 203:			**Date:**	

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.